Revised 4/22/04

Digitizer Card FPGA Internal Registers (Byte Count)[Bits] ~136 bytes

Channel 0		Address (A7-A0) 00-FF
4 [32]	Fast Sum Threshold R/W	00-03
4 [32]	Slow Sum Threshold R/W	04-07
4 [32]	Very Slow Sum Threshold R/W	08-0B
2 [16]	Imediate Threshold R/W	0C-0D
4 [32]	Fast Sum Latched R	20-23
4 [32]	Slow Sum Latched R	24-27
4 [32]	Very Slow Sum Latched R	28-2B
2 [16]	Mode select R/W	2C-2D
2 [16]	MADC Manual setting R/W	2E-2F
2 [16]	Current reading R	30-31
Channel 1		
4 [32]	Fast Sum Threshold R/W	40-43
4 [32]	Slow Sum Threshold R/W	44-47
4 [32]	Very Slow Sum Threshold R/W	48-4B
2 [16]	Imediate Threshold R/W	4C-4D
4 [32]	Fast Sum Latched R	50-53
4 [32]	Slow Sum Latched R	54-57
4 [32]	Very Slow Sum Latched R	58-5B
2 [16]	Mode select R/W	5C-5D
2 [16]	MADC Manual setting R/W	5E-5F
2 [16]	Current reading R	60-61
General		
2 [16]	Fast Sum Length R/W	F0-F1
2 [16]	Slow Sum Length R/W	F2-F3
2 [16]	Very Slow Sum Length R/W	F4-F5
2 [16]	TBT Ram Pointer R	F6-F7
2 [16]	FPGA Control Register R/W	F8-F9
Channel 2		70-9F
Channel 3		A0-DF

Revised 4/21/04

Timing Card FPGA Internal Registers (Byte Count)[Bits] ~46 bytes

Clocks/Timing		Address (A7-A0) 00-FF
4 [32]	Real Time Clock R/W	00-03
4 [32]	Microseconds Counter R/W	04-07
8 [64]	Fast Latch Time Stamp	08-0B
8 [64]	Slow Latch Time Stamp	0C-0F
8 [64]	Very Slow Latch Time Stamp	10-13
Controller		
2 [16]	Fast Sum Length R/W	20-21
2 [16]	Slow Sum Length R/W	22-23
2 [16]	Very Slow Sum Length R/W	24-25
1 [8]	Sample Devisor R/W	26
1 [8]	State Number W	28
Communications		
1[8]	TCLK Event FIFO R	30
2 [16]	MDAT Event Data R	32-33
General		
1[0]	Force Clear W	F0
1[0]	Force Start W	F1
1[0]	Force Stop W	F2

Revised 4/21/04

ACC Card FPGA Internal Registers (Byte Count)[Bits] ~64 bytes

Masks		Address (A7-A0) 00-FF
1 [5]	Abort Mask R/W	00
2 [16]	Imediate Abort Masks R/W	02-03
2 [16]	Fast Abort Masks R/W	04-05
2 [16]	Slow Abort Masks R/W	06-07
2 [16]	Very Abort Masks R/W	08-09

Multiplicities		
1 [4]	Imediate Multiplicity R/W	0A
1 [4]	Fast Multiplicity R/W	0B
1 [4]	Slow Multiplicity R/W	0C
1 [4]	Very Slow Multiplicity R/W	0D

General		
1[5]	Force Abort W	F0
1[5]	Force Abort Permit W	0F

HV/MADC Card FPGA Internal Registers (Byte Count)[Bits] ~64 bytes

HV		Address (A7-A0) 00-FF
2 [16]	HV Setting R/W	00-01
2 [16]	HV ReadBack R	02-03
2 [16]	HV Return Readback R	04-05

MADC		
2 [16]	MADC Setting W	08-09

BLM Abort Settings Table

Each State:

1 byte State Number
2 bytes Abort Mask Imediate
2 bytes Abort Mask Fast
2 bytes Abort Mask Slow
2 bytes Abort Mask Very Slow
32 Bytes Imediate Threshold
64 Bytes Fast Threshold
64 Bytes Slow Threshold
64 Bytes Very Slow Threshold
4 Bytes Abort Multiplicity

19 Bytes Spares

256 Bytes Total

256 States:

64k bytes total setup space.

BLM Backplane DIN connector Signal Definition J2

	A1	B1	C1
1	A0	+5V	GND
2	A1	GND	+15V
3	A2	NC	+15V
4	A3	NC	GND
5	A4	NC	ABORT0
6	A5	NC	ABORT1
7	A6	NC	ABORT2
8	A7	NC	ABORT3
9	A8	NC	GND
10	A9	NC	AbortCS0
11	A10	NC	AbortCS1
12	A11	GND	AbortCS2
13	A12	+5V	AbortCS3
14	GND	NC	AbortCS4
15	MREQ*	NC	Fast_LATCH(0)
16	MEMRD*	NC	Slow_LATCH(1)
17	WR*	NC	V Slow_LATCH(2)
18	GND	NC	GND
19	D0	NC	AIP
20	D1	NC	RESET DC
21	D2	NC	RESET
22	D3	GND	MAKE_MEAS
23	D4	NC	CPU Detect
24	D5	NC	GND
25	D6	NC	BusReq
26	D7	NC	BusAck
27	GND	NC	GND
28	IRQ0	NC	-15V
29	IRQ1	NC	-15V
30	IRQ2	NC	GND
31	IRQ3	GND	OSC
32	+5V	+5V	+5V
	A32	B32	C32

Red = CPU 1 and CPU 2 Cards

Blue = Daughter cards

Revised 6/21/04